DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-8 in the reply filed on 16 Oct. 2007 is acknowledged.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. Figure 1-3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, are rejected under 35 U.S.C. 102(b) as being anticipated by US 20030203575 to Hung et al.

Regarding claim 1, Hung discloses a semiconductor device in fig. 3-9, comprising: a semiconductor substrate (100); a nonvolatile memory cell (area I) that includes a memory transistor realized by a MOS transistor including a memory gate oxide (108) film that is arranged on the semiconductor substrate (100), and a floating gate (FG) made of polysilicon [0038] that is arranged on the memory gate oxide film (108) which floating gate (FG) is in an electrically floating state; and a selection transistor (SG) realized by a MOS transistor that is serially connected to the memory transistor, fig. 2, the selection transistor (SG) including a selection gate oxide film (108) that is arranged on the semiconductor substrate (100), and a selection gate (110a) made of polysilicon [0038] that is arranged on the selection gate oxide film (108); and a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film (108) that is arranged on the semiconductor substrate (100), and a peripheral circuit gate (110b) made of polysilicon that is arranged on the peripheral circuit gate oxide film (108), fig. 7B; wherein the memory gate oxide film (108) is arranged to be thinner than the peripheral circuit gate oxide film (memory gate oxide 108 = 90 A^{o}, high voltage gate oxide = 200 A^{o}, [0037]).

Regarding claim 3, Hung discloses the semiconductor device as claimed in claim 1, wherein the selection gate oxide film and the memory gate oxide film

are arranged to have a same thickness (same layer 108 under FG and SG), fig. 9A.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 20030203575 to Hung et al.

Regarding claim 2, Hung fails to disclose wherein the memory transistor and the selection transistor are PMOS.

However, at the time the invention was made; it would have been obvious to a person having ordinary skill in the art to modify transistor of Hung to make a PMOS transistor, because making either NMOS or PMOS transistor is well know in the art by using the N-type or P-type dopants.

Regarding claim, Hung fails to disclose the semiconductor device as claimed in claim 1, wherein the selection gate oxide film and the peripheral circuit gate oxide film are arranged to have a same thickness.

However, at the time the invention was made; it would have been obvious to a person having ordinary skill in the art to modify the thickness teaching Hung as claimed because it has been held that where the general conditions of the claims are discloses in the prior art, it is not

inventive to discover the optimum or workable range by routine experimentation, MPEP 2144.05, and adjusting the gate dielectric thickness in order to obtain an intended work function is well known in the art, see Ding (US 7238575) col. 2 lines 25-30.

8. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 20030203575 to Hung et al. in view of US 6282123 to Mehta

Regarding claim 5, Hung fails to disclose the semiconductor device further comprising: a capacitor including a lower electrode made of polysilicon that is arranged on the semiconductor substrate via an insulating film, and an upper electrode made of polysilicon that is arranged on the lower electrode via a capacitor insulating film; and the capacitor insulating film is arranged on an upper surface and a side surface of the floating gate.

However, Mehta discloses a semiconductor device in fig. 8A-B comprising a capacitor (with dielectric 150) including a lower electrode (140) made of polysilicon that is arranged on the semiconductor substrate (120) via an insulating film (160), and an upper electrode (170) made of polysilicon, col. 6 line 2, that is arranged on the lower electrode (140 via a capacitor insulating film (150); and the capacitor insulating film (150) is arranged on an upper surface and a side surface of the floating gate (140). At the time the invention was made; it would have been obvious to a person having ordinary skill in the art to add the capacitor teaching of Mehta to the semiconductor device of Hung in order to create an

EEPROM or nonvolatile memory device and such memory structure is typical in the art.

Regarding claims 6-8, the combination of Hung and Mehta disclose the semiconductor device wherein the peripheral circuit gate (110b) and the upper electrode, selection gate (110a), the floating gate (FG), and the lower electrode are created from a same polysilicon layer.

The limitation "created from the same polysilicon layer" in claims 5-8 are considered to be process limitation that do not carry weight in a claim drawn to structure, MPEP 2113.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

29 Oct. 2007

/Thao X Le/
Primary Examiner, Art Unit 2814